Abstract

A test methodology which provides that test structures, such as transistors, are arranged in a plurality of rows. A logic circuit controls which row is to be measured. An incrementer receives a triggering signal and functions as an address adder. Each time the triggering signal rises from 0 to 1, the output of the incrementer increases by 1. The output of the incrementer serves as the address input into a decoder. The decoder is connected to the rows of test structures. Preferably, each test structure contains a control circuit which is controlled by this signal (i.e., the output of the decoder). If the test structures are transistors, bias to each of the transistors can be applied separately with a common gate, source and well, and measurement can be done with a separate drain node.